SPECIFICATION AMENDMENTS

At page 1, lines 1-2, please amend the Title as follows:

~~MICROPROCESSOR WITH HARDWARE CONTROLLED POWER MANAGEMENT~~ PIPELINED DATA PROCESSOR WITH SIGNAL-INITIATED POWER MANAGEMENT CONTROL

At page 1, between lines 2 and 3, please insert the following:

RELATED APPLICATIONS

This is a division of U.S. patent application no. 10/216,615, filed August 9, 2002.

At page 1, lines 4-6, please amend the text of the section entitled "Technical Field of the Invention" as follows:

This invention relates in general to integrated circuits, and more particularly to a ~~microprocessor having hardware controlled~~ pipelined data processor with power management control.

At page 4, lines 3-21, please amend the text of the section entitled "Summary of the Invention" as follows:

~~In accordance with the present invention, a method and apparatus is provided which provides significant advantages in reducing the power consumption of a microprocessor.~~

~~In the present invention, a processing unit includes a plurality of subcircuits and circuitry for generating a clock signal thereto. Circuitry is provided for detecting the assertion of a control signal; responsive to the control signal, disabling circuitry disables the clock signal to one or more of the subcircuits.~~

~~The present invention provides significant advantages over the prior art. A significant reduction in the power consumed by a computer may be effected by disabling the clock to the microprocessor circuitry. The present invention allows the disabling and enabling of the microprocessor clock signals to be controlled by a single control signal. Further, an acknowledge signal may be provided to notify external circuitry of the suspended state of the microprocessor.~~

In accordance with the presently claimed invention, a pipelined data processor with signal-initiated power management control is provided in which a plurality of subcircuits, including pipeline subcircuitry, and circuitry for generating and controlling at least one clock signal are responsive to at least one control signal by selectively disabling a clock signal to the pipeline subcircuitry.

In accordance with one embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, control circuitry, clock circuitry and a plurality of subcircuits. The plurality of interface electrodes includes one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The control circuitry is coupled to the one or more control electrodes and responsive to the one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination. The clock circuitry is coupled to the control circuitry and responsive to the at least one clock control signal by providing at least a first clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes, the control circuitry and the clock circuitry, and includes pipeline subcircuitry responsive to the first clock signal by selectively operating on one or more instructions for data

processing. A first portion of the pipeline subcircuitry is responsive to the active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to the active first clock signal by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, controller means, clock source means and subcircuit means. The interface means is for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The controller means is for responding to the one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination. The clock source means is for responding to the at least one clock control signal by generating at least a first clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively. The subcircuit means includes pipeline means for responding to the first clock signal by selectively operating on one or more instructions for data processing. A first portion of the pipeline means is for responding to the active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline means is for responding to the active first clock signal by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an

apparatus including integrated processor circuitry includes a plurality of interface electrodes, control circuitry, clock circuitry and a plurality of subcircuits. The plurality of interface electrodes includes one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The control circuitry is coupled to the one or more control electrodes and responsive to the one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states. The clock circuitry is coupled to the control circuitry and responsive to the at least one clock control signal by providing at least a first clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the inactive state following the first incoming control signal states combination. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes, the control circuitry and the clock circuitry, and includes pipeline subcircuitry responsive to the first clock signal by selectively operating on one or more instructions for data processing. A first portion of the pipeline subcircuitry is responsive to the active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to the active first clock signal by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, controller means, clock source means and subcircuit means. The interface means is for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states

corresponding to a power management operation mode. The controller means is for responding to the one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states. The clock source means is for responding to the at least one clock control signal by generating at least a first clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the inactive state following the first incoming control signal states combination. The subcircuit means includes pipeline means for responding to the first clock signal by selectively operating on one or more instructions for data processing. A first portion of the pipeline means is for responding to the active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline means is for responding to the active first clock signal by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, control circuitry, clock circuitry and a plurality of subcircuits. The plurality of interface electrodes includes one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The control circuitry is coupled to the one or more control electrodes and responsive to the one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination. The clock circuitry is coupled to the control circuitry and responsive to the at least one clock control signal by providing at least a

first clock signal having an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to the at least one clock control signal de-assertion and assertion states, respectively. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes, the control circuitry and the clock circuitry, and includes pipeline subcircuitry responsive to the first clock signal by selectively operating on one or more instructions for data processing. A first portion of the pipeline subcircuitry is responsive to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, controller means, clock source means and subcircuit means. The interface means is for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The controller means is for responding to the one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination. The clock source means is for responding to the at least one clock control signal by generating at least a first clock signal having an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to the at least one clock control signal de-assertion and assertion states, respectively. The subcircuit means includes pipeline means for responding to the first

clock signal by selectively operating on one or more instructions for data processing. A first portion of the pipeline means is for responding to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline means is for responding to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, control circuitry, clock circuitry and a plurality of subcircuits. The plurality of interface electrodes includes one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The control circuitry is coupled to the one or more control electrodes and responsive to the one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states. The clock circuitry is coupled to the control circuitry and responsive to the at least one clock control signal by providing at least a first clock signal with an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the inactive state following the first incoming control signal states combination. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes, the control circuitry and the clock circuitry, and includes pipeline subcircuitry responsive to the first clock signal by selectively operating on one or more instructions for data processing. A first portion of the pipeline subcircuitry is responsive to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of

one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, controller means, clock source means and subcircuit means. The interface means is for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The controller means is for responding to the one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states. The clock source means is for responding to the at least one clock control signal by generating at least a first clock signal with an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the inactive state following the first incoming control signal states combination. The subcircuit means includes pipeline means for responding to the first clock signal by selectively operating on one or more instructions for data processing. A first portion of the pipeline means is for responding to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and a second portion of the pipeline means is for responding to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, control circuitry, clock circuitry and a plurality of subcircuits. The plurality of interface electrodes includes one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The control circuitry is coupled to the one or more control electrodes and responsive to the one or more incoming control signals and a first clock signal by providing at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination. The clock circuitry is coupled to the control circuitry and responsive to the at least one clock control signal by providing the first clock signal having active and inactive states substantially independent of the at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes, the control circuitry and the clock circuitry, and includes pipeline subcircuitry responsive to the active second clock signal by executing one or more instructions for data processing.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, controller means, clock source means and subcircuit means. The interface means is for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The controller means is for responding to the one or more incoming control signals and a first clock signal by generating at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-

assertion states with the respective assertion states following the first incoming control signal states combination. The clock source means is for responding to the at least one clock control signal by generating the first clock signal having active and inactive states substantially independent of the at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively. The subcircuit means includes pipeline means for responding to the active second clock signal by executing one or more instructions for data processing.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, control circuitry, clock circuitry and a plurality of subcircuits. The plurality of interface electrodes includes one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The control circuitry is coupled to the one or more control electrodes and responsive to the one or more incoming control signals and a first clock signal by providing at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states. The clock circuitry is coupled to the control circuitry and responsive to the at least one clock control signal by providing the first clock signal having active and inactive states substantially independent of the at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the second clock signal inactive state following the first incoming control signal states combination. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes, the control circuitry and the clock circuitry, and includes pipeline subcircuitry responsive to the active second clock signal by executing one or more instructions for data

processing.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, controller means, clock source means and subcircuit means. The interface means is for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode. The controller means is for responding to the one or more incoming control signals and a first clock signal by providing at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states. The clock source means is for responding to the at least one clock control signal by generating the first clock signal having active and inactive states substantially independent of the at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the second clock signal inactive state following the first incoming control signal states combination. The subcircuit means includes pipeline means for responding to the active second clock signal by executing one or more instructions for data processing.

At page 19, lines 3-8, please amend the text of the section entitled "Abstract of the Disclosure" as follows:

~~A processing unit includes a plurality of subcircuits and circuitry for generating clock signals thereto. Detection circuitry detects the assertion of a control signal and disabling circuitry is operable to disable the clock signals to one or more of the subcircuits responsive to the control signal.~~ A pipelined data processor with signal-initiated power management control in which a plurality of subcircuits, including pipeline subcircuitry, and circuitry for generating and controlling at least

one clock signal are responsive to at least one control signal by selectively disabling a clock signal to the pipeline subcircuitry.